## REMARKS

### Present Status of the Application

The Office Action dated January 28, 2003 rejected claims 1-15 under 35 USC 103(a) as being unpatentable over the prior art principally relied upon the admitted prior art, Wakabayashi et al (JP 59-054249), Mukai et al. (US Patent No. 5,391,915), Liu (US Patent No. 6,486,535), and Corisis et al. (US Patent No. 6,215,177). Furthermore, the drawings were objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the reference numeral 209 (FIG. 3) not mentioned in the description.

The remarks set forth in the Office Action have been carefully considered. The specification has been amended to include a proper reference of the numeral sign 209. In addition, claims 1, 8, 10 and 15 have been amended to more clearly distinguish over the prior art. In view of the above amendment and the following discussion, the Applicant earnestly solicits reconsideration and allowance of all the pending claims.

### Discussion of the Office Action Objections

The Office Action objected to the drawings as failing to comply with 37 CFR 1.84(p)(5) because they include the reference sign 209 not mentioned in the description.

As submitted above, the paragraph [0016] has been amended to include a proper reference to the reference sign 209. Reference sign 209 indicates a portion of the tie bars 208 that is downwardly bent to down-set the die pad 204. It is believed that the drawings now are in proper form, and withdrawal of the objection is respectfully requested.

**Discussion of the Office Action Rejections**

Discussion of the claim rejection under 35 USC 103

1. The Office Action rejected claims 1-3, 5, 7 and 8 under 35 USC 103(a) as being unpatentable over the admitted prior art in view of Wakabayashi et al. and Mukai et al. This rejection is respectfully traversed.

As described in amended claims 1 and 8 (and shown in FIG. 3), the invention teaches a leadframe structure that specifically includes a plurality of first leads that define a chip-bonding region in which a *die pad is arranged at a sideways biased location.* A greater gap thereby is left between the die pad and the leads, so that the second leads can further extend and terminate in contact pads in the chip-bonding region to advantageously allow the placement of several passive devices.

None of the cited references teach or suggest the specific arrangement of the die pad as described above.

As shown in FIG. 1, the admitted prior art teaches a die pad that clearly is not placed at a *sideways biased location.* Wakabayashi et al. discloses a leadframe package structure in which a chip is mounted on a die pad. As shown in the drawings, the die pad in Wakabayashi et al. is neither placed at a sideways biased location in a chip-bonding region as defined in the claims. Mukai et al. further discloses a package structure that does not include any leadframe structure or die pad. Outside the above deficient references, none of the other cited references (including Liu and Corisis et al. as discussed hereafter) either adequately disclose or suggest the arrangement of the die pad at a sideways biased location, as recited in the claims.

Moreover, none of the references recognize the advantages of the present invention. In the present invention, because the position of the die pad is biased, different contact pads can be arranged in the chip-bonding region for carrying more passive devices. This arrangement enables the integration of more than one passive device within the package structure, thus improving electrical properties of the package structure.

For at least the above reasons, it is submitted that claims 1 and 8 patently distinguish over the prior art references. Claims 2, 3, 5 and 7, being dependent upon patentable claim 1, should be also patentable over the prior art references.

2. The Office Action rejected claim 4 under 35 USC 103(a) as being unpatentable over the admitted prior art in view of Wakabayashi et al. in view of Liu. This rejection is respectfully traversed.

First, pursuant to the recent amendments to 35 U.S.C. § 103(c), Applicants respectfully submit that it is inappropriate to use the Liu patent as a cited reference. The Liu patent is owned by Advanced Semiconductor Engineering, Inc., which is the same assignee of the present invention. Therefore, pursuant to 35 U.S.C. § 103 (c), the Liu patent "shall not preclude the patentability" of the present invention. Applicants will be happy to submit a terminal disclaimer, if deemed necessary or appropriated.

As discussed above, the admitted prior art and Wakabayashi et al. are fully deficient to teach or suggest the claimed invention in which *the die pad is arranged at a sideways biased location in the chip-bonding region.* On the other hand, Liu teaches a leadframe structure in which passive elements are bonded and connected between the leads and/or between the lead and the

die pad of the leadframe. As shown in the drawings, Liu neither teaches nor suggest the placement of the die pad at a sideways biased location in the chip-bonding region, as recited in the claims. Only describing a specific leadframe structure, Liu further neither suggests the implementation of the invention in a quad flat package, as further specified in claim 4.

For at least the above reasons, it is submitted that claim 4 patently distinguishes over the cited references.

3. The Office Action rejected claims 6, 9-11, 14, and 15 under 35 USC 103(a) as being unpatentable over the admitted prior art and Wakabayashi et al. in view of Corisis et al. This rejection is respectfully traversed.

As discussed above, the admitted prior art and Wakabayashi et al. are deficient to teach or suggest the claimed invention in which *the die pad is arranged at a sideways biased location in the chip-bonding region* (this limitation is also recited in amended claims 10 and 15). Though Corisis et al. may suggest the use of an adhesive tape as recited in the claims, it however shows the same deficiencies as the other references and fails to specifically teach or suggest *the arrangement of the die pad at a sideways biased location of the chip-bonding region.* Therefore, even if they are combined with one another, these references would have failed to adequately meet the claimed invention as recited in claims 10 and 15.

For at least the above reasons, it is submitted that claims 6, 9, 10 and 15 are patentable over the prior art references.

Claim 12 is believed allowable for at least the same reasons as discussed above in connection with claim 4, and claim 13 being dependent upon patentable claim 10 should be also

allowable.

For at least the foregoing reasons, all pending claims patently define over the cited references, either alone or in combination. Accordingly, the rejection under §103 should be withdrawn.

## CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-15 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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## VERSION WITH MARKED-UP AMENDMENTS TO SHOW THE AMENDMENTS MADE

**In The Specification:**

Please amend the specification as follows.

**[0016]** As conventionally arranged, tie bars 208 connecting the die pad 204 to the leadframe 200 support the die pad 204. The tie bars 208 prevent the die pad 204 from bending when an encapsulating process is subsequently performed. A portion 209 of the tie bars 208 further may be downwardly bent to down-set the die pad 204.

**In The Claims:**

1. (Amended) A packaging structure integrating passive devices, comprising:

a leadframe, wherein the leadframe includes a plurality of first leads defining a chip-bonding region, a plurality of second leads extending and terminating in a plurality of contact pads within the chip-bonding region, and a die pad located at a sideways biased position in the chip-bonding region;

a chip bonded onto the die pad;

at least a passive device mounted between and connected to the contact pads;

a plurality of bonding wires electrically connecting the chip, the passive device, and the first and second leads to one another; and

an encapsulant material encapsulating the chip, the passive device, and the bonding wires.

8. (Amended) A leadframe structure suitable for use in a chip packaging structure, the leadframe structure comprising:

a plurality of first leads defining a chip-bonding region in the leadframe structure;

a plurality of second leads extending and terminating in a plurality of contact pads within the chip-bonding region; and

a die pad arranged at a sideways biased position in the chip-bonding region.

10. (Amended) A packaging structure integrating passive devices, comprising:

a leadframe, wherein the leadframe includes a plurality of first leads defining a chip-bonding region, a plurality of second leads extending and terminating in a plurality of contact pads within the chip-bonding region, and a die pad located at a sideways biased position in the chip-bonding region;

an adhesive tape bonded to bottom surfaces of the contact pads;

a chip bonded onto the die pad;

at least a passive device mounted between and connected to the contact pads;

a plurality of bonding wires electrically connecting the chip, the passive device, and the leads to one another; and

an encapsulant material encapsulating the chip, the passive device, and the bonding wires.

15. (Amended) A leadframe structure suitable for use in a chip packaging structure, the leadframe structure comprising:

a plurality of first leads defining a chip-bonding region in the leadframe structure;

a plurality of second leads extending and terminating in a plurality of contact pads within the chip-bonding region;

an adhesive tape bonded to bottom surfaces of the contact pads; and

a die pad arranged at a sideways biased position in the chip-bonding region.